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Design and Development of Symmetrical Super-Lift DC-AC Converter using Firefly Algorithm for Solar-Photovoltaic Applications

Johny Renoald ALBERT[1], *Albert Alexander STONIER*[2]*

[1] *Department of Electrical and Electronics Engineering, Assistant professor, Vivekanandha college of Engineering for Women, Namakkal, Tamilnadu, India.*
[2] *Department of Electrical and Electronics Engineering, Professor, Kongu Engineering College, Erode, Tamilnadu, India.*
* *E-mail: jorenoeee@gmail.com*

Abstract: The super-lift technique is an exceptional contribution to DC-DC conversion technology. A replacement approach of Symmetrical Super-Lift Multilevel Inverter (SSLMLI) DC/AC technology is proposed with reduced number of elements compared with the traditional multilevel inverter (MLI). In this method, the firefly algorithm (FA) conveys a leading task for the super-lift multilevel inverter (SLMLI) topology for solar-photovoltaic application. It generates low distortion output and consumes the harmonic band of the Fast Fourier Transform (FFT) framework by the employment of proposed algorithm. The simulation circuit for fifteen level output uses single switch super-lift inverter feed with different kinds of load (R, RL & RLE) conditions. The power quality is improved in super-lift multilevel inverter with minimized harmonics underneath the various modulation index (MI) while varied from 0.1 up to 0.8. The circuit is designed in a field programmable gate array which includes the firefly rule to help the multilevel output, to reduce the lower order harmonics and finds the best switching angle. As a result, minimum Total Harmonic Distortion (THD) from simulation and hardware circuit is achieved. Due to the absence of bulky switches, inductor and filter elements expose the effectiveness of the proposed system.

1 Introduction

The requirement for sustainable energy has grown up significantly over the years due to the fast depletion of fossil fuel and also the greenhouse effect. The solar cell PV module growth in India within the year 2016-17 ranged from 2000 to 2022MW and in the future, it would be 5000 to 5500MW due to the growing demand for the energy is needed [1]. The DC to AC conversion techniques will be separated into 2 types: Multilevel Modulation (MLM) and Pulse-width Modulation (PWM). Each of this modulation schemes has a different mechanism for providing the voltage level [2]. In general, there are three sorts of traditional multilevel inverters structures like Neutral point clamped (NPC) [3], flying capacitor (FC) [4] and cascaded H Bridge multilevel inverters (CHBMLI) [5] which are notably helpful to extend the output voltage level. Over the past few years, the several multilevel inverters are proposed for DC-AC conversion to solar-PV Systems to achieve 15 level MLI with different load condition [6, 7], This conventional solar multilevel inverters are requires 28 switches and in binary, trinary mode 12 switches can be obtained. Whereas as in MMC (Multilevel Modular Conventional) method only 7 switches are employed to achieve 15 level [8, 9]. In the cascade symmetric multilevel inverter, Charles Ikechukwu odeh et al., 2015 [10], the each module is made up of H- and half bridges, two isolated equal dc sources and a bidirectional auxiliary circuit. The reduction of the Total Harmonic Distortion (THD) in multilevel inverters requires resolution of complex nonlinear transcendental equations with Firefly algorithm is proposed Mehdi Belkacem et al., 2017 [11]. In recent Marif Daula Siddique et al., 2019 [12], MLI topology has been proposed with the basic unit requires three dc voltage sources and ten switches to synthesize 15 levels across the load. The symmetrical 15 level MLI, Belwin Edwards et al., 2018 [13] present the DC source magnitudes are equal and the results are verified in RL load condition both simulation and hardware approach, which vertically routines a reference waveform to achieve the desirable multilevel output waveform. The above perceptions are applicable for industrial and commercial applications like Flexible AC Transmission System devices and AC drives. The disadvantages of conventional converter topology is to integrate many levels using several clamping diodes, clamping capacitor, bulky Filters and DC sources and may extend the establishment zone because of increase in built cost of the converter and convoluted control circuits. In symmetrical MLI technique, all the DC sources contain a unique quality which guarantees great modularity and it is the same quantity of DC voltage that is applied to the subsequent stage of the converter circuit. This multilevel inverting strategy horizontally collect levels to get the output waveform (e.g., a sine wave). The system is designed with 15-level SLMLI along with optimum control techniques like a firefly algorithmic (FA) rule to find the effective switching angle and THD values that compare with more than asymmetrical MLI [14, 15]. The SLMLI uses seven capacitors C_6, C_7, C_8, C_9, C_{10}, C_{11}, and C_{12} which are used to split or divide the output voltage into fifteen levels created by single pole multi- through (SPMT) and double pole double through switch - 2P2TS shown in Fig. 1. As a result, the proposed method increases the output voltage gain with modulation index limitation and reduces voltage drop across the switch (S_1-S_2) that is comparatively beyond that of the conventional multilevel inverters. The proposed model of super-lift inverter is well suits for reactive power compensation and providing desired alternating staircase output wave. The quality of the end result voltage has been improved by the numerous voltages with the assistance of least semiconductor switches. The symmetrical super lift multilevel strategy utilizes single MOSFET switch and capacitor energy banks on the grounds that solar PV source voltage might be broadened and this may create a higher incentive in output voltage by way of increasing the level.

The number of node voltages are from V_7 up to V_1. The purpose of the capacitor voltage (E_m) for each capacitor is to function as the

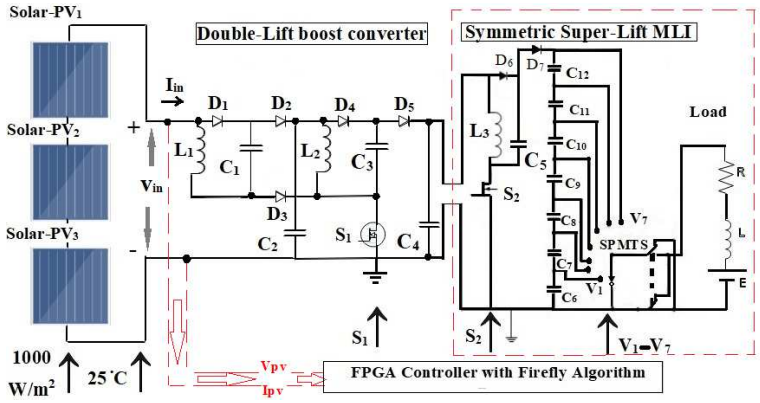


Fig. 1: Circuit diagram for fifteen levels symmetric super-lift multilevel inverter (SLMLI).

capacitor energy bank.

$$Em = \frac{Vdc}{N-1} \tag{1}$$

where N denotes number of levels.

The capacitor band switch or single pole multi-through switch (SPMTS) Turn on positive charging output terminal voltage from V_7, V_6, V_5, V_4, V_3, V_2, V_1, V_0 and negative discharging output terminal voltage turn off are -V_1, -V_2 -V_3, -V_4, -V_5, -V_6, & -V_7 respectively in SLMLI . It has been furthermore analyzed and developed by using MATLAB / Simulink software. The hardware implementation of FPGA is better power quality improvement with FA support of finding the best THD and switching angle values. The prototype model suits to reactive compensation and present inverter circuit minimizes electromagnetic interference problem with the help of main capacitor bank (C_6-C_{12}), and it is used in medium and low power applications, particularly in renewable power electronics utility.

2 DOUBLE-LIFT BOOST CONVERTER

The double lift boost (DLB) converter is modified form of step up boost converter. It consists of a coupled inductor, charge pump and active clamper circuits which are more complicated [16]. Here, the same method is adapted, show that output voltage is twice greater than the input voltage source, but with the necessity of reducing module structure in the double-lift boost circuit.

The input voltage source (V_{in}) for the converter is roughly around 42V, when the capacitor voltage V_{C1} is charged by input source (V_{in}), in the stable state (Voltage across capacitor) $V_{C1} = V_{input}$ and the voltage V_1 across the capacitor C_2 is,

$$V_1 = \frac{2-K}{1-K} V_{in} \tag{2}$$

The capacitor voltage V_{C3} is charged by V_1. When current passing through inductor L_2 with increased voltage V_1, switch (S_1) is in ON mode (KT). When it decreases with the voltage level - (Vout - 2Vinput), during the switch (1-k) T off period, the ripple of the inductor current (iL_2) is,

$$\triangle\, iL_2 = \frac{V_1}{L_2} KT + \frac{V_0 - 2V_1}{L_2} I_{L1} (1-K) T \tag{3}$$

$$V_o = \frac{2-K}{1-K} = \left(\frac{2-K}{1-K}\right)^2 V_{in} \tag{4}$$

Where K is the duty cycle and the voltage transfer gain;

$$G = \frac{V_0}{V_{in}} = \left(\frac{2-K}{1-K}\right)^2 \tag{5}$$

The variation ratio of current iL_1through inductor L_1 is,

$$\xi 1 = \frac{\Delta i_{L1}/2}{i_{L1}} = \frac{K(2-K)TV_{in}}{2L_1I_0} = \frac{K(1-k)^2}{2(2-k)^3} = \frac{R}{fL_1} \tag{6}$$

The variation ratio of current iL_2 through inductor L_2 is,

$$\xi 1 = \frac{\Delta i_{L1}/2}{i_{L1}} = \frac{K(1-K)TV_1}{2L_2I_{in}} = \frac{K\,TV_0\,(1-K)^2}{2(2-K)^3 L_2 I_0}$$
$$= \frac{K(1-K)^2}{2(2-K)} \frac{R}{fL_2} \tag{7}$$

Therefore, the variation ratio of output voltage V_0 is

$$\varepsilon = \frac{\Delta V_0/2}{V_0} = \frac{k}{2Rfc_4} \tag{8}$$

The maximum induced voltage and currents from MPP passing through the next stage of converters are provided. The performance of DLB converter yields the output voltages of (Vout) 120V which was developed by two important parameters, namely inductors (L_1,L_2) and capacitors (C_1,C_2 & C_3).

3 PV SOURCE AND MODULATION SCHEME

Solar photovoltaic (PV) panels are a versatile energy technology that can help electrical customers of all kinds with their electricity needs. There are two main categories of solar panel installation: 1.Grid connected PV, 2. Standalone PV. They are primarily differ in size and location, and also are unique in several other system characteristics. PV installations may be residential, commercial or industrial, utility-scale, ground-mounted, rooftop mounted, and wall mounted or floating etc., [17, 18]. The need of several sources on the DC side of the converter makes multilevel technology attractive for photovoltaic applications. In this regards, a solar super-lift multilevel inverter is a standalone off-grid Balance of System (BOS) component of a photovoltaic module [19, 20] and it can be used in off grid systems like Electric vehicles and R, RL & RLE load connected system [21–23]. The BOS encompasses all components of a photovoltaic system other than the photovoltaic panels. This includes wiring, switches, a mounting system, a battery bank, battery charger and one or many solar multilevel inverters etc.,

This type of solar super-lift multilevel inverters have special functions adapted for use with photovoltaic arrays, includes maximum power point tracking. In the photovoltaic arrays (SPV_1-SPV_3) the terminal voltage is not equal to the constant maximum power point (MPP). The Fig.2 is shows that maximum voltage of any one out of three solar panel. The three PV modules are adjusted to fit the characteristics measured standard test condition with irradiation key parameters like 1000 W/m^2, temperature 25^{o}C, and nominal operating cell temperature 45^{o}C. The MPP parameter for open circuit

Table 1 Comparission of fifteen level traditional MLI Vs symmetric super-lift MLI.

MLI	Total Number of Stages	Total Number of Main diodes	Total Number of Switches	Total Number Of clamping Diodes	Total Number of DC bus Capacitor	Total Number of Balancing Capacitors
NPC	7/15 level	6/28	6/28	10/182	0/14	6/0
FC		0/28	6/28	6/0	5/14	6/91
CHB		0/12	12/28	12/0	3/7	0/0
Proposed SLMLI		2/2	1/1	2/2	3/14	1/1

voltage is (22.1V*3) 66.3V and short-circuits current is 5.96A as shown in Table 2. The Perturb and Observe rule is supported to generate the duty cycle as well as maximum power (Pmax) efficiency in PV module. The basic expression for maximum efficiency (η) of a photovoltaic cell is given by the ratio of output power to the incident solar power. (Radiation flux times area (A))

$$\eta = \frac{P_{max}}{E.A_{cell}} \tag{9}$$

The input sources from solar PV are connected with the double-lift boosted DC-DC converter which works and lifts up a voltage which is encouraged into the super lift multilevel inverter. The simulation method of Solar-PV array modules are used in sun power SPR 305- WHT and the number of cells per module using 96 cells (i.e., 96*0.21V=20V). The solar cell module two connections are followed by the combination of series and parallel connected module. The solar PV array module is normally designed as Solar-PV1, Solar-PV2, and Solar-PV3 made by supply (20V*3) 60V and 4.25 A. The solar super-lift inverters (SSLI) differ from conventional inverters, as an individual super-lift inverters is attached to one are more number of solar panel. This can improve the overall efficiency of the system. When the panel output voltage is lowered due to cloudy condition during checking of PV-module in day time, the MPP (P&O) controller is adjusts the voltage by a small amount from the array open circuit voltage 22.1V and short-circuits current is 5.96A.
Record-low temperature: -10^{o}C
Temperature coefficient of (V_{OC}): - (0.30) % /^{o}C
Module open circuit voltage (V_{OC}): 20 V
Inverter maximum input voltage: 60 V

The STC temperature is 25^{o}C. This temperature needs to be deducted from the array location's record-low temperature of -10 degrees as follows:

25 - (-10) = 35^o difference.

Multiply the 35^o difference by the temperature coefficient of VOC, then multiply by the module's V_{OC}:

35 $\times$ 0.0030 = 0.105,
0.105 $\times$ 20V = 2.1V

The number of PV module will be increase due to record-low temperatures. After adding the increase in voltage to Module VOC, then divide the inverter maximum input voltage by single PV module Voc. This will gives the maximum number of modules that can be wired in a series string per that inverter and specific location.

2.1V+20V = 22.1Vmax
60V / 22.1 = 2.71 (Round down to a whole number)

The maximum number of modules in this series string is 2.71. A series string of 3 could potentially produce more than 60V during record-low temperatures. The quantity of modules wired in series multiplied by the Vmax equals to maximum system voltage

3$\times$22.1 = 66.3 V Maximum PV module voltage.

The modulation scheme of Perturb and observe rule is maintained to create the duty cycle of both the converter and also the SSLMLI. The aim of MPP rule is to incorporate a variety of upper, lower limit (D-max) values and incremental step-by-step values (Delta-D) which help to find the most effective optimum converter duty cycle (D). The pulse generator using firefly matlab functions are fed in to both DLB converter and SLMLI switches in Fig. 3. The FA algorithmic program has performed varying the modulation index across the multilevel inverter switches, herewith producing appropriate SLMLI output and THD values.

Table 2 Deviation report of PV- module with/without MPPT.

Description	Without MPPT using SLMLI	With MPPT using SLMLI
Maximum power (Pmax)	69-70 watts	75 watts
Voltage at Pmax (Vmp)	20V	21.1V
Current at Pmax (Imp)	4.25A	4.96A
Open-circuit voltage (Voc)	21.5V	22.1V
Short-circuit current (Isc)	4.51A	5.96A

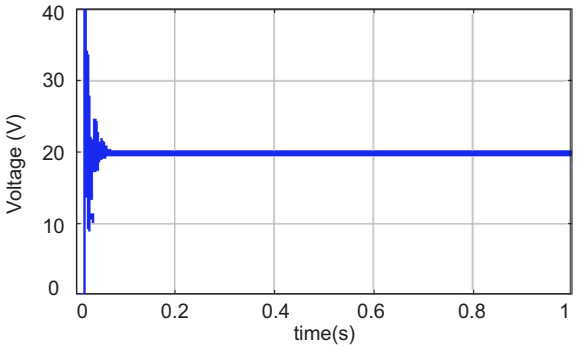


Fig. 2: Solar -PV DC output voltage

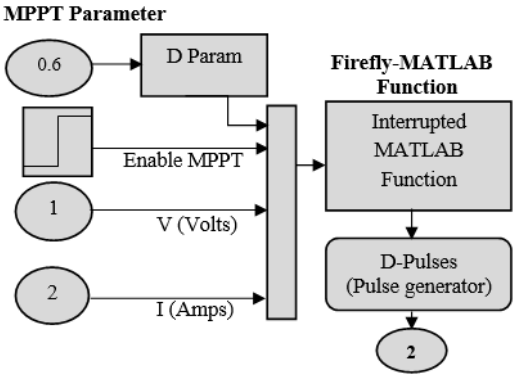


Fig. 3: MPPT with firefly controller Function

4 SYMMETRICAL SUPER-LIFT MULTILEVEL INVERTER

An approach has been created with super-lift multilevel inverter (SLMLI) which constructed from modified Voltage -lift Luo (DC/DC) converter [24]. The input sources from solar-PV are fed with double-lift boost DC-DC converter, which is operated maximize DC voltage fed into a super lift multilevel inverter. The multilevel electrical converter based on DC sources leads in two cases:

1.Symmetrical type MLI 2. Asymmetric type MLI

The asymmetric MLI has been investigated a maximum number of levels obtained with a high number of switches and gate driver circuits for generating all levels [25]. Here, symmetric multilevel inverter minimum number of levels is applied to achieve maximum output voltage. The solar-PV system is used three numbers of (Solar-PV_1 up to Solar-PV_3) modules. The symmetrical SLMLI consists of single MOSFET switch S_2, and main capacitor C_6-C_{12} combined with SPMT (Single Pole Multi Through) switch. As the most important part in SLMLI, the number of required switches against the required voltage level is an extremely important element with in the design. In this regards, the SLMLI produces a large number of multilevel outputs is increased by using multiple capacitors without increasing the number of bridges or power circuit topology. The advantage of this proposed topology is that it's less number of apparatus and reduced voltage stress across the main capacitor bank.

4.1 Modified super-lift multilevel inverter design

This module consists of only one MOSFET Switch, 2 freewheeling diodes and 7 parallel main switching capacitors to generate fifteen level output (+7V, 0 & -7V), (+6V, 0 & -6V), (+5V, 0 & -5V), (+4V, 0 & -4V), (+3V, 0 & -3V), (+2V, 0 & -2V), (+ 1V, 0 & -1V), whereas traditional multilevel inverters NPC, FC and CHB require twenty-eight switches to generate the fifteen levels output is shown in Table 1. Several levels used for increasing multiple capacitors to achieve maximum output voltage to attain less THD. A number of the capacitor devices are connected in series so that the voltage stress across the devices could be reduced. With this, connection formulated symmetrical multilevel (DC-AC) inverter number of levels has been increased as mentioned below, where C indicates the number of capacitors adding with single switch used in the proposed super lift multilevel inverter suitable & particularly for Solar PV renewable energy application.

$$N\text{level} = 2C + 1$$

Proposed circuit,

$$N \text{ level} = 2(7) + 1 \text{ switch} = 15 \text{ level} \quad (10)$$

$$2(3 \text{ Capacitor}) + 1S = 7 \text{ level} \quad (11)$$

$$2(10 \text{ Capacitor}) + 1S = 21 \text{ level} \quad (12)$$

$$2(12 \text{ Capacitor}) + 1S = 25 \text{ level} \quad (13)$$

$$2(17 \text{ Capacitor}) + 1S = 35 \text{ level} \quad (14)$$

$$2(22 \text{ Capacitor}) + 1S = 45 \text{ level} \quad (15)$$

Here, fifteen level super-lift MLI can be applied. When the main switch S_2 is on, the inductor (L_3), and capacitor (C_5) are charged by the source voltage ($V_{DCinput}$) during switch on period kT. The end result voltage V_{out} is highly raised from the source voltage because of inductor L_3 and capacitor C_5, when the main switch during off period (1-k) T decreases voltage level -(V_{out} -2V_{input}). This symmetric MLI operates in single pole multi through switch with different load conditions. The amount of voltage increases, when the harmonic content of the voltage is decreased. Therefore ripple current of the inductor iL equation can be given as,

$$\nabla iL1 = \left(\frac{Vin}{L}\right) KT = \left[\frac{Vo - 2Vin}{L}\right] KT \quad (16)$$

5 SUPER-LIFT MULTILEVEL INVERTER MODES OF OPEARTION

5.1 ON-state multilevel inverter

The output voltage switch position (V_7) is in charging mode, when it is at the node in between D_7 (diode) and C_{12} (capacitor), there will be a potential voltage across the capacitor Vc_{12}.which is named as V_7 =+1/7 V_{dc} under the condition, 2P2T switch is closed as shown in Fig. 4. It is taken as the exact charging output voltage for positive half cycle of the load. The same process should be followed,

- V_6= +1/6V_{dc} when it is at the node in between the capacitor C_{12} and C_{11}, there will be a potential voltage across the capacitor Vc_{11}.
- V_5= +1/5V_{dc} when it is at the node in between the capacitor C_{11} and C_{10}, there will be a potential voltage across the capacitor Vc_{10}.
- V_4= +1/4V_{dc} when it is at the node in between the capacitor C_{10} and C_9, there will be a potential voltage across the capacitor Vc_9.
- V_3= +1/3Vdc when it is at the node in between the capacitor C_9 and C_8, there will be a potential voltage across the capacitor Vc_8.
- V_2= +1/2Vdc when it is at the node in between the capacitor C_8 and C_7, there will be a potential voltage across the capacitor Vc_7.
- V_1= +1/1Vdc when it is at the node in between the capacitor C_7 and C_6, there will be a potential voltage across the capacitor Vc_6

and finally the single pole multi through switch (SPMTS) is at a point V_0. V_0 = 0 (neutral) when it is at the node in between C_6 and V_0, there will be a potential voltage across the output will be followed through 2P2T switch that will be passing to the next state of load. The symmetric Super-Lift MLI Switching methods are shown in Table 3.

5.2 OFF-state multilevel inverter

The output voltage switching position (-V_1) is in discharging mode, when it is at the node in between N(neutral) and C_6, there will be potential drop across the capacitor -Vc_6, which is named as -V_1= -1/V_{dc} and under the condition, 2P2T switch is closed as shown in Fig. 5. It is taken as the exact discharging output voltage for the negative half cycle of the load. The same process should be followed,

- -V_2= -1/2V_{dc}, when it is at the node in between the capacitor C_6-C_7, there will be a potential drop across the capacitor (-Vc_7).
- -V_3= -1/3V_{dc}, when it is at the node in between the capacitor C_7-C_8, there will be a potential drop across the capacitor (-Vc_8).
- -V_4= -1/4V_{dc}, when it is at the node in between the capacitor C_8-C_9, there will be a potential drop across the capacitor (-Vc_9).
- -V_5= -1/5V_{dc}, when it is at the node in between the capacitor C_9-C_{10}, there will be a potential drop across the capacitor (-Vc_{10}).
- -V_6= -1/6V_{dc}, when it is at the node in between the capacitor C_{10}-C_{11}, there will be a potential drop across the capacitor (-Vc_{11})

and finally the single pole multi through switch (SPMTS) is at a point (-V_7). -V_7= -1/7V_{dc}, when it is at the node in between the capacitor C_{11}-C_{12}, there will be a potential drop across the capacitor (-Vc_{12}). It will be followed 2P2T switch and passing through the next state of load.

6 Implementation of firefly algorithm

The interpreted MATLAB function of firefly algorithmic program developed by Xian she yang in 2007-2008, which was made on

Table 3 Inverter Switching Method of Fifteen level SLMLI.

S.No	Switch terminal output voltage Point (SPMTS)	Modes of operation ON	Switch ON state	Switch terminal output voltage point (SPMTS)	Modes of operation OFF	Switch OFF state
1.	V_7	I	+1/7 V_{dc}	-V_7	XV	-1/7 V_{dc}
2.	V_6	II	+1/6V_{dc}	-V_6	XIV	-1/6 V_{dc}
3.	V_5	III	+1/5 V_{dc}	-V_5	XIII	-1/5 V_{dc}
4.	V_4	IV	+1/4 V_{dc}	-V_4	XII	-1/4 V_{dc}
5.	V_3	V	+1/3 V_{dc}	-V_3	XI	-1/3 V_{dc}
6.	V_2	VI	+1/2 V_{dc}	-V_2	X	-1/2 V_{dc}
7.	V_1	VII	+1/1 V_{dc}	-V_1	IX	-1/1 V_{dc}
8.	V_o	VIII	0	-V_0	VIII	0

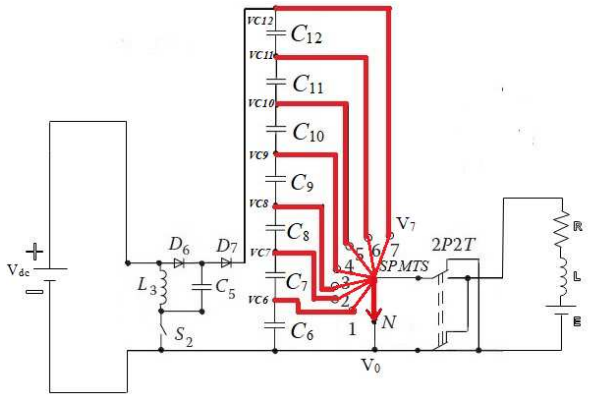


Fig. 4: ON-state Super-lift multilevel inverter.

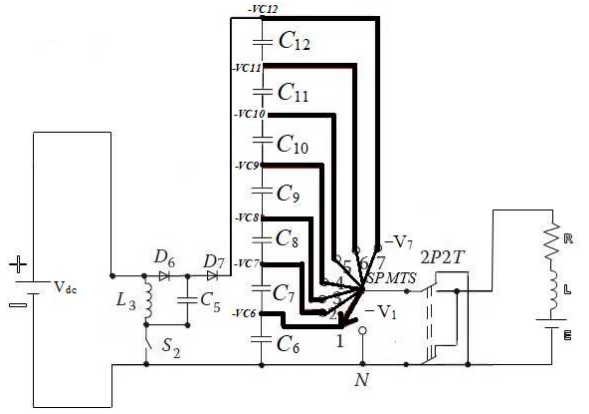


Fig. 5: OFF-state Super-Lift Multilevel Inverter.

flashing patterns and behavior of firefly. It is basic to attract mating partners to seek out the best solution among the population and generate pulses of both double boost converter and SSLMLI. The firefly rule can deal with non-linear and multimodal optimization issues. It does not use the velocity function and there are no issues as those associated with GA and PSO.

Step 1: **Initialization** In the initial process, the PV current and voltage are initialized the algorithm parameters such as β_0, n, α, γ, (population size) N and the termination criterion. Here, the firefly initial position is assumed to be a switching angle of the multilevel converter. In addition, the brightness of every firefly is taken as generated solar (PV) power P_{pv} 20V, corresponding to the position of this firefly. The fireflies are two fundamental functions such as generate bioluminescence flashes to draw in matting partners and to draw in potential prey. The Initialize objective function is,

$$I(r) = \left(\frac{I_s}{r^2}\right) \tag{17}$$

where I(r) is the intensity of source, r is the observers distance from the source.

Step 2: Brightness Evaluation In this second step, the multilevel converter is operated based on the updated position of each and every firefly in sequential order. For each switching angle, the corresponding PV output power, Ppv is taken as the brightness or light intensity of the respective firefly. This step is repeated for the position of all fireflies in the population. Now determine the light intensity of each of the fireflies to find out the brightness of every firefly.

$$I = I_0 e^{-\gamma r^2} \tag{18}$$

If we tend to take the absorption coefficient γ into account. The light intensity I vary with the square of the distance r.

Step 3: Update the Position of Fireflies & Termination The firefly with better brightness remains in its position and the remaining other fireflies update their position. Terminate the program, if the termination criterion is reached. Otherwise, attend the step one. The optimization firefly algorithm rule is terminated once the dislocation of all fireflies in consecutive steps attained a predefined set reduce value. Once the program is terminated, the initialize firefly population by considering the subsequent equation,

$$x_{t+1} = x_t + \beta_0\, e^{-\gamma r^2} + \alpha\varepsilon \tag{19}$$

Where the second term is because of the attraction and third term is randomization with being the randomization parameters. Calculate the Attractiveness of Firefly is,

$$\beta = \beta_0\, e^{-\gamma r^2} \tag{20}$$

Movement of few brighter fireflies towards brighter one, the movement of Firefly I is attract to a different additional attractive (brighter) firefly. J is the determine by,

$$x_i = x_i + \beta_0\, e^{-\gamma r i,j}(xj - xi) + \alpha\varepsilon \tag{21}$$

Finally, update the light-weight intensives of firefly and rank the fireflies. Once ranking of the fireflies, find the current optimum solution is shown in Fig.6. In the following Table 4, the firefly implementation values of Matlab/Simulink platform has been given below.

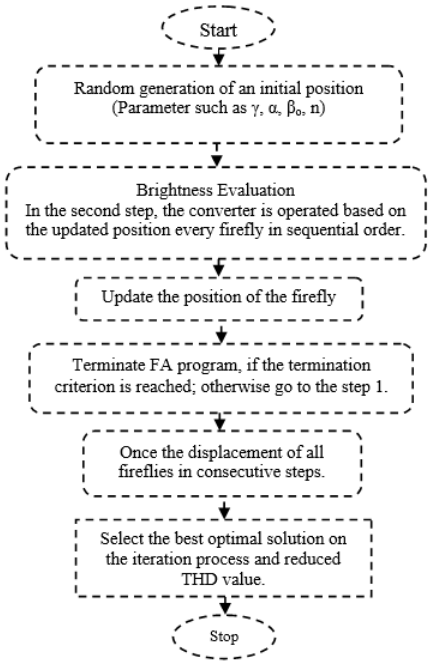


Fig. 6: Procedure of Firefly Algorithm applies to minimal THD reduction.

Table 4 Implementation parameters of firefly algorithm.

Descriptions	Values
Maximum generation (γ)	10
Population (p)	20
Alpha (α)	1
Attractiveness (β_o)	50
Number of fireflies (n)	100

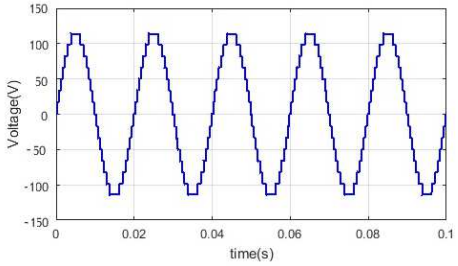


Fig.7 a. Output voltage waveform R

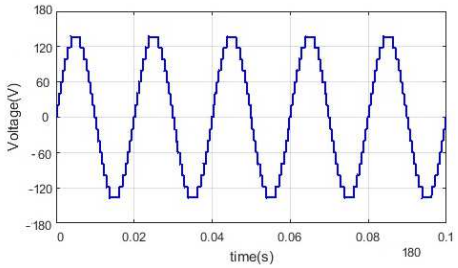
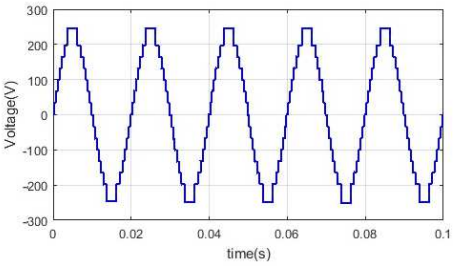


Fig.7 b. Output voltage waveform RL



c

Fig. 7: **c.** Output voltage waveform RLE load

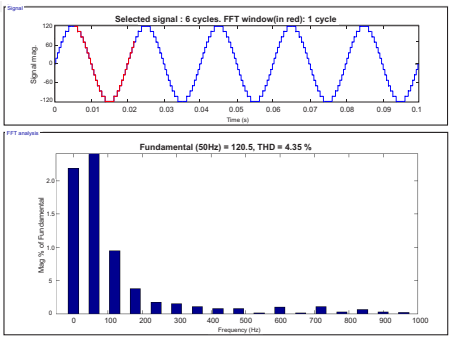


Fig.8 a. THD Analysis R

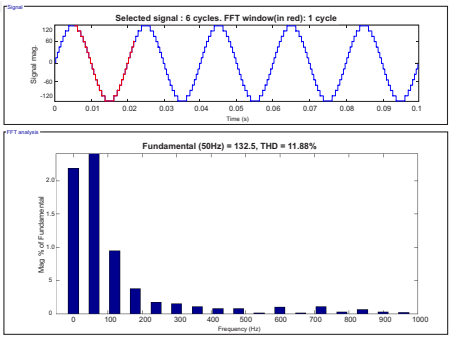
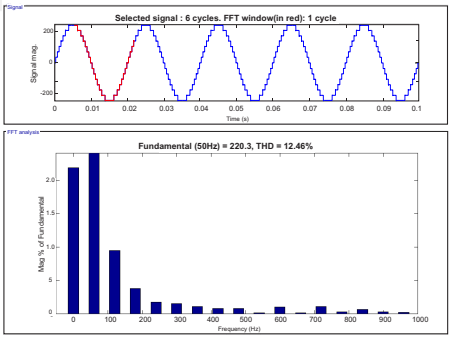


Fig.8 b. THD Analysis RL



c

Fig. 8: **c.** THD Analysis RLE load.

7 SIMULATION RESULT AND DISCUSSION

The paper deals with fifteen levels symmetrical form of SLMLI assist firefly algorithmic program by using Matlab/Simulink code.

Table 5 Simulation parameter of symmetric type of super-lift MLI.

S.no	Parameter Name	Range
1.	Open circuit voltage (V_{oc})	66.3V
2.	Short circuit current (I_{sc})	5.96A
3.	Inductor	560 mh
4.	Capacitor (DC-DC)	1500μF
5.	Capacitor bank (DC-AC)	2600μF
6.	R load	30Ω
7.	RL load	30Ω, 40mH
8.	RLE load	30Ω, 40mH, 220V

The code will realize the optimum modulation index (MI) solution that depends on the switching angle of SLMLI. The individual input supply (PV) is directly connected to double boost converter and it's a series connected into a multilevel inverter. This SLMLI simulation is performed with the output frequency of 50 Hz and a switch frequency of 5000 Hz. Their corresponding SLMLI electrical converter output voltage R, RL and RLE are shown in Fig. 7(a,b,c). The THD level obtained here is 4.35% R load in Fig 8a, 11.88% RL load in Fig 8b and 12.46% of RLE load in Fig 8c. The simulation parameters of SLMLI as shown in Table 5.

The FA is a much higher attainment level economically to find the best switching angle related to different load Vs THD level presented in Table 6. The ranges of MI vary from 0.1 up to 0.8 for corresponding switching angles are evaluated with firefly formula presented (section 6). The speed of convergence of firefly program for obtaining THD gives a very high performance within the chance of finding the global optimizing solution associated with both GA and PSO as discussed [26–28]. The Firefly algorithm used to reduce THD, however there is increase in potential level which is compared with earlier results of metaheuristic non-linear and discrete optimization algorithms were approached and verified [29, 30]. In our proposed work, the MPPT using symmetrical super-lift MLI is associated with firefly implementation as compared with the existing methodology. The parameters are shown in firefly algorithm (FA) maximum generation 10, population 20 and number of firefly 100, it was quit updated the light intensives of ranking the firefly and the optimum solution is found with minimum time of interval (Table 7). In the earlier Firefly approach of symmetrical 15 level inverter has a low THD level which is significantly decrease 22% - 16% [31]. In our proposed symmetric 15 level MLI with reduced THD level around minimum level 4.35% (R Load), 11.88% (RL load) and 12.46% (RLE load) has been presented. The main drawback of non-linear loads is generation of harmonic current in addition to the original AC current. In the Non linear load the distortion level increases in RL and RLE load conditions is due to the change of impedance value across the load. The improvement of reactive power (VAR) variation in the RL & RLE load by eliminating the negative sequence discharging current in the MLI with help of DC-link capacitor unit in order to keep the stable system.

8 Hardware result and discussion

The SLMLI is used to test Firefly Algorithmic (FA) rule tuned with FPGA control signal access to operate RLE motor load condition shown in Fig. 9. The (MPP) maximum power point voltage given by Photovoltaic cells ranges are based on the atmospheric situations. The ideal voltage levels are not received while the modulation index movements are under a critical limit. In case there are 15-level symmetric multilevel inverters, the critical value of the modulation index is 0.8. When the modulation index moves above that value, the switches turn into the lower voltage, therefore symmetrical super-lift multilevel inverters are turned off.

The values of modulation index (MI) are calculated from the below equation (22).

$$MI = \left(\frac{V_{ref}}{V_{carrier}}\right) \tag{22}$$

Table 6 THD Analysis of R, RL and RLE

Modulation Index	Optimization Tuning	THD (%)			Optimum Switching angle with modulation index (MI)	(Load) THD%	Minimum magnitude of Even and Odd harmonics [up to 25^{th} order for 15 level MLI]
		RLE	RL	R			
0.8		29.46	21.88	19.35	α_1=18.95, α_2=21.50	R load	1^{st} -0.12 (Odd)
0.7		**12.46**	12.74	13.92	α_3=33.91 (MI=0.45)	4.35 %	20^{th} -0.05 (Even)
0.6		14.39	14.65	11.81			
0.5	**FA**	15.79	16.22	17.76	α_1=16.05, α_2=19.21	RL load	7^{th} -0.02 (Odd)
0.4		16.00	15.50	**9.35**	α_3=31.54 (MI=0.27)	11.88%	10^{th} -0.10 (Even)
0.3		17.19	13.80	15.90			
0.2		19.21	**11.88**	16.01	α_1=5.37, α_2=19.21	RLE load	5^{th} -0.28 (Odd)
0.1		21.99	18.16	18.15	α_3=43.54 (MI=0.72)	12.46%	18^{th} -0.18 (Even)

Table 7 Performance Analysis Optimum Success Rate of FA, GA & PSO.

Algorithms/Functions		Number of Particles	Time Taken	GA	PSO	FA
Michalewicz (d =16)	[32]	50	2	95%	98%	99%
Rosenbrock (d =16)	[33]	50	6	90%	98%	99%
Dejong (d = 256)	[34]	50	7	100%	100%	100%
Schwefel (d = 128)	[35]	50	4	95%	97%	100%
Ackley (d = 128)	[36]	50	4	90%	92%	100%
Rastrigin	[37]	50	2	77%	90%	100%
Easom	[38]	50	4	92%	90%	100%
Griewang	[39]	50	1	90%	92%	100%
Shubert (d = 18)	[40]	50	2	89%	92%	100%
Yang (d = 16)	[41]	50	2	83%	90%	100%
Proposed (SSLMLI)		100	2	86%	95%	99%

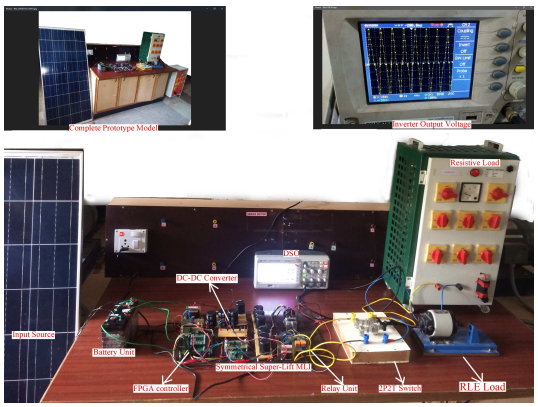


Fig. 9: Proposed FPGA Xilinx-3 AN Kit assist symmetrical SLMLI photography view.

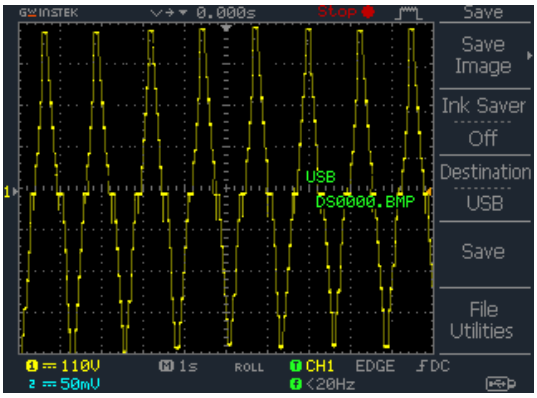


Fig. 11: Prototype multilevel output of Symmetrical Super-lift inverter.

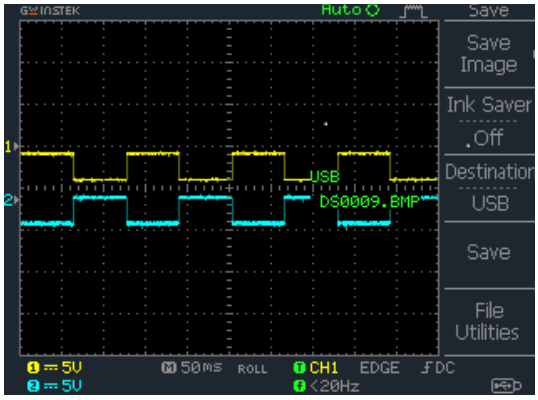
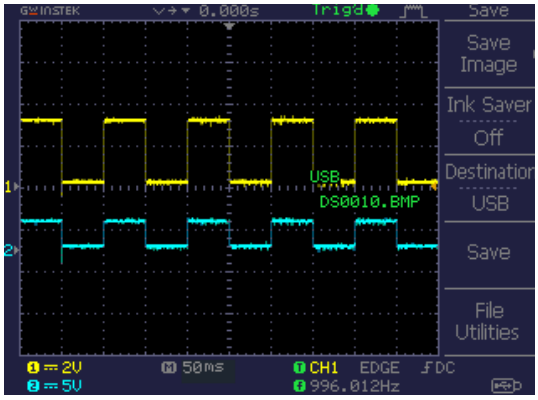


Fig. 10: **a.** Relay unit pulses- positive half cycle 1



b

Fig. 10: **b.** Relay unit pulses- negative half cycle 2

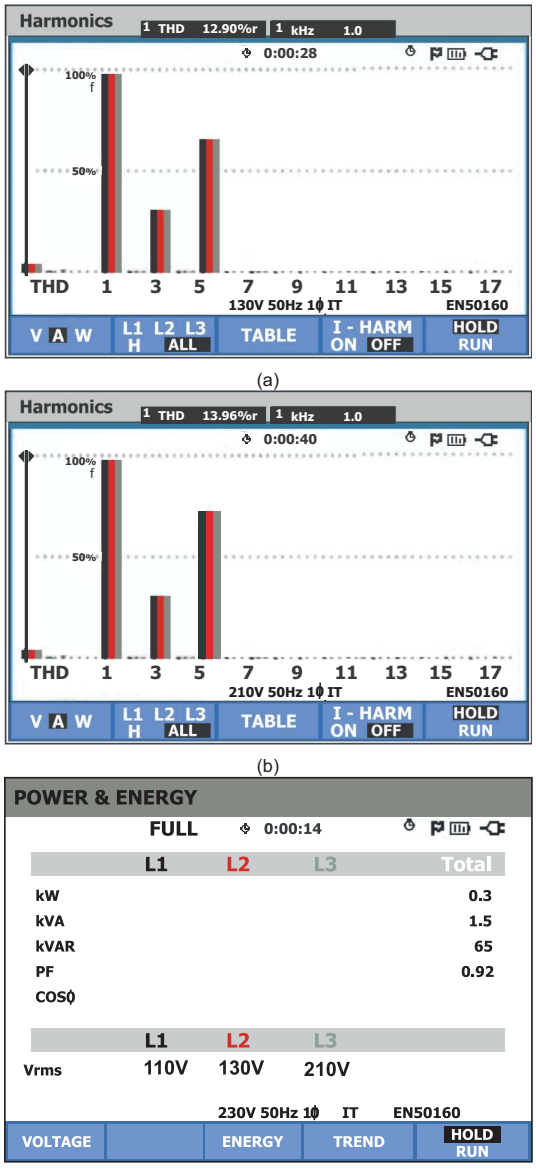


Fig. 12: THD spectrum of experimental output voltage.

The PV parameter is chosen as open circuit voltage of 20V and short circuit current of 1.3A (Single PV-string). The prototype is verified under working day time. The MPP ranges are based on the irradiance and temperature variations.

In general, the DC-DC converter consists of one MOSFET switch (S_1) operating frequency range at 1 kHz and proposed multilevel inverter uses only single MOSFET switch (S_2) where pulses form FPGA board clock frequency up to 50 MHz. The Xilinx Spartan 3AN kit is verified VHDL program assist with firefly algorithm. The voltage across the switching diodes of both DLB converter and SLMLI is 0.7V. This prototype model of SLMLI is turning on MOSFET-IRFP460 through the voltage in series and along with

Table 8 Comparison between Experimental and simulated values of THD SSLMLI strategies.

S.no	Simulation output voltage with different load condition					
1.	R Load (THD %)	Vrms	RL Load (THD %)	Vrms	RLE Load (THD %)	Vrms
	4.35	120 V	11.88	132 V	12.46	220 V
	Hardware output voltage with different load condition					
2.	R Load (THD %)	Vrms	RL Load (THD %)	Vrms	RLE Load (THD %)	Vrms
	5.96	110 V	12.90	130 V	13.96	210 V

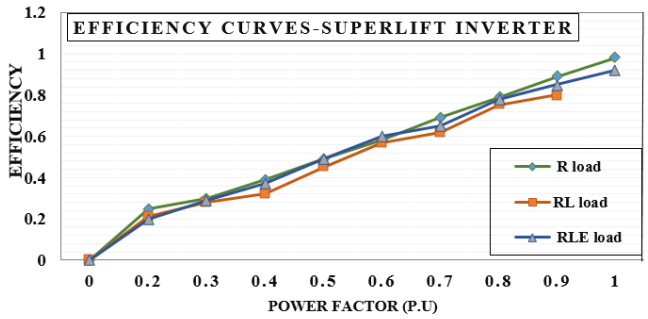


Fig. 13: Proposed SLMLI efficiency curves.

main capacitor bank (1500μF) or SLMLI capacitor bank C_6-C_{12}. The first half cycle positive sequence is made up with electronic relay (KEMET-EE2 series) double pole double through switch (2P2T) unit. The relay unit pulses are functioning at 50 ms and the operating frequency from 20 Hz to 996 Hz as shown in Fig. 10(a, b). The same process is to be continued from main capacitors (C_6-C_{12}) during negative phase sequence, they are discharged by the double pole double through relay unit switch. This type of electronic relay uses multiple contacts suitable for electronic switching system and low magnetic interference benefits. These relay units have the maximum capacity of 60W, 2A. The RLE load across the SLMLI output voltage as shown in Fig. 11.

The results of staircase output voltage is obtained as 210V for RLE motor load condition, 130V for RL load and 110V for R Load, with the support of firefly algorithm. The reactive power will be enhanced from 50VAR to 65VAR in different type of operational load condition. It gives Minimum THD value of 13.96%, 12.90% & 5.96% in the bandwidth of spectrum varying from 1 kHz to 5 kHz as shown in Fig. 12 and Table 8. The reactive power is to support the electrical system, when renewable PV system is integrated with the off-grid, capacitive, resistive, and inductive load. The proposed SLMLI efficiency curves (R, RL, and RLE load) are shown in fig.13. However, the THD level is increase in RL, RLE load due to the absence of filter components. The blocking voltage across each semiconductor device must be minimized with main capacitor bank. Its helps to generate reactive power to meet the demand of the inductive loads. This will keep that reactive power from having to flow all the way from the utility to the loads (RL, RLE).The optimum switching angle is produced from firefly program to assist the load voltage with minimized THD, at the same time much development of power factor improvements.

The voltage lifting technique DC/DC is successfully employed in Super-Lift Multilevel Converter [42–44]. Where the conversion is generally focused arithmetic (or) geometric progression in power series, the aim of this function is multiple repeating parts. To validate this proposed model 15 level case reduce devices have been developed and it minimizes switching stress with low distortion output. Therefore, Symmetrical SLMLI stage grows up to 21, 25, 35, & 45 level series, the output voltage furthermore varies to reduce total harmonic distortion using medium and low power applications.

9 Conclusion

In this paper, fifteen level symmetrical form of super-lift MLI has been applied with firefly algorithm and FPGA strategy equipment, which results in minimal distortion of an output voltage and power quality improvement. In the SLMLI, the productive output voltage and performance factors such as harmonic minimum distortion values are analyzed. The contrast obtained when comparing hardware and simulation is, the value of 4.35% THD in simulation model and 12.90% THD in hardware model.

The validity of the simulated results is tested by single phase fifteen levels firefly assist FPGA prototype model with the effect of less switching stress and minimal electromagnetic interference. In the simulation and hardware implementation, the ± 10 voltage deviation from R and RLE load is due to the variation of Load and absence of filter components, which reduce the cost of the inverter circuit. The total harmonic distortion values in RL & RLE load and the power factor values of R, RLE load condition were almost the same. The reactive power is developed 65.38 VAR effectively in RL load condition due to the power consumed by inductance and main capacitor bank unit, in order to keep the system to be balanced. The symmetrical super-lift multilevel inverter notion will soon to be a great choice for power electronic frameworks, particularly for solar- Photovoltaic applications.

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